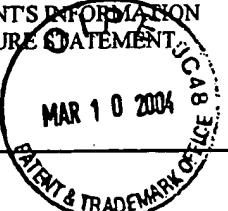


ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	STRUCTURE AND METHOD FOR LOCAL RESISTOR ELEMENT IN INTEGRATED CIRCUIT TECHNOLOGY																																																																																		
<p>Application Number : 10/1708023 Confirmation Number: First Named Applicant: Jason Gill Attorney Docket Number: BUR920030118US1 Art Unit: 2826 Examiner: Kevin Quinto Search string: (5232865 or 5330930 or 5665629 or 5930638 or 6117792 or 20030116820 or 20020003311).pn</p>																																																																																			
<h3>US Patent Documents</h3> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>5232865</td><td>1993-08-03</td><td>Manning et al.</td><td></td><td></td><td></td></tr><tr><td>1</td><td>2</td><td>5330930</td><td>1994-07-19</td><td>Chi</td><td></td><td></td><td></td></tr><tr><td>1</td><td>3</td><td>5665629</td><td>1997-09-09</td><td>Chen et al.</td><td></td><td></td><td></td></tr><tr><td>1</td><td>4</td><td>5930638</td><td>1999-07-27</td><td>Reedy et al.</td><td></td><td></td><td></td></tr><tr><td>1</td><td>5</td><td>6117792</td><td>2000-09-12</td><td>Kitagawa</td><td></td><td></td><td></td></tr></tbody></table> <h3>US Published Applications</h3> <p>Note: Applicant is not required to submit a paper copy of cited US Published Applications</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Pub. No.</th><th>Date</th><th>Applicant</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>20030116820</td><td>2003-06-26</td><td>Daubenspeck et al.</td><td></td><td></td><td></td></tr><tr><td>1</td><td>2</td><td>20020003311</td><td>2002-01-10</td><td>Uematsu</td><td></td><td></td><td></td></tr></tbody></table> <p>Signature</p> <table border="1"><tr><td>Examiner Name</td><td>Date</td></tr><tr><td>Kevin Quinto</td><td>9/3/09</td></tr></table>								init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	1	1	5232865	1993-08-03	Manning et al.				1	2	5330930	1994-07-19	Chi				1	3	5665629	1997-09-09	Chen et al.				1	4	5930638	1999-07-27	Reedy et al.				1	5	6117792	2000-09-12	Kitagawa				init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass	1	1	20030116820	2003-06-26	Daubenspeck et al.				1	2	20020003311	2002-01-10	Uematsu				Examiner Name	Date	Kevin Quinto	9/3/09
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	Applicant: Gill et al		
	Filing Date: Herewith 02/03/04		Group: 2826

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
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<i>RZ</i>	AJ	JP4151825A	05/25/1992	Japan	HO1L	21/28	Abstract only
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	AL						
	AM						

OTHER DOCUMENTS

<i>RZ</i>	AN	"VERTICALLY INTEGRATED LOAD RESISTOR FOR MOS STATIC RAM CELLS", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pgs. 5675-5677
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	AP	
	AQ	
	AR	

Examiner: *Kevin Quinby*

Date Considered:

9/3/04

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